R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

IN THE DRAWINGS

Applicants' submit herewith a replacement sheet showing the amended FIG. 4 as approved by the Examiner (see item 11 on form PTOL-326 in paper no. 5).

SUPPORT FOR AMENDMENTS TO THE SPECIFICATION

The specification has been amended for consistency. Support for the amendments to the specification can be found in the drawings as originally filed, for example, on FIGS. 3-5 and in the claims as originally filed, for example, claim 13. As such, no new matter has been introduced.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 3-5, in the claims as originally filed, for example, claims 2 and 13, and in the specification as originally filed, for example, on page 1, lines 11-14, on page 3, lines 1-6, on page 4, line 14 through page 5, line 1, and on page 7, line 7 through page 8, line 13 and on page 9, line 10 through page 10, line 8. In particular, FIG. 5

shows a plurality of delay devices 109a-109n. Each of the delay devices 109a-109n presents one of the claimed delay times. The signal DIN_DLY is presented to register 102, which is clocked by the signal CLK. In this example, the signal DOUT can change states (e.g., go from low-to-high or high-to-low) when the register 102 captures the state of the signal DIN_DLY upon each transition of the signal CLK. Each of the delay times is less than a period of the signal CLK to provide a configurable setup/hold window for the input of the register 102 relative to a transition of the clock signal CLK. No new matter has been added.

OBJECTION TO THE SPECIFICATION

The objection to the specification under 35 U.S.C. §112, first paragraph, for failing to support the subject matter set forth in the claims is respectfully traversed and should be withdrawn.

The objection to the specification is unclear as to whether the objection is based upon the written description portion of 35 U.S.C. §112, first paragraph, or the enablement portion of 35 U.S.C. §112, first paragraph. In particular, the Office Action states the test for the written description portion of 35 U.S.C. §112, first paragraph (see page 2, paragraph no. 2 of the Office Action), but ends the objection with the conclusory statement "the specification does not provide **an enabling disclosure** to support

[the] claimed limitation" (see page 2, paragraph no. 2 of the Office Action, emphasis added).

With respect to the written description portion of 35 U.S.C. §112, first paragraph, the Office Action fails to meet the Office's burden to factually establish a reasonable basis to question the adequacy of the written description provided for the presently claimed invention (MPEP §2163.04). Specifically, the Office Action fails to present any evidence or convincing line of reasoning why a person skilled in the art would not recognize in the specification a description of the invention defined by the claims (see page 2, paragraph no. 2 of the Office Action; see also MPEP §2163.04 citing *In re Wertheim*).

With respect to the enablement portion of 35 U.S.C. §112, first paragraph, the Examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention (see MPEP §2164.04 (citing *In re Wright*)). The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation (see MPEP §2164.01 (citing *United States v. Teletronics, Inc.*)). The Office Action fails to meet the Office's burden to factually establish a reasonable basis to question the enablement provided for the presently claimed invention. Specifically, the Office Action fails to present any evidence or

convincing line of reasoning why one reasonably skilled in the art would not be able to make or use the invention from the disclosures in the specification coupled with information known in the art without undue experimentation (see page 2, paragraph no. 2 of the Office Action; see also MPEP §2164.01).

In contrast to the position taken in paragraph no. 2 of the Office Action that "the specification, as originally filed does not provide support for the invention as now claimed" and "the specification does not provide an enabling disclosure to support this claimed limitation," one reasonably skilled in the art (i) would recognize in the specification a description of the invention defined by the claims and (ii) could make or use the invention from the disclosures in the specification coupled with information known in the art without undue experimentation (see MPEP §§ 2163.04 and 2164.01). In particular, the drawings (e.g., FIGS. 4 and 5) and specification as originally filed clearly provide a written description (see *Vas-Cath, Inc. v. Mahurkar*) that would allow one reasonably skilled in the art (i) to recognize in the specification a description of the invention defined by the claims and (ii) to make or use the invention from the disclosures in the specification coupled with information known in the art without undue experimentation. For example, both FIG. 4 and FIG. 5 show a plurality of delay elements 109a-109n. FIG. 5 provides an example of the delay elements comprising a number of gates (e.g., buffers,

inverters). Further supporting disclosure can be found on page 7, lines 6-19 of the specification, as originally filed, which state:

> **The switch 111 may select at least one of the outputs of the delay circuits 109a-109n.** The switch 111 may select the appropriate delay circuit 109a-109n in response to the signal S_H. The signal S_H may be implemented **to provide any appropriate delay** in order to meet the criteria of a particular implementation. Additionally, the signal S_H may be generated by any appropriate type device and/or configuration in order to meet the criteria of a particular implementation. The switch 111 may have an output 140 that may present the signal DIN_DLY. The switch 111 may allow the circuit 100 to provide an optimal data setup-hold window. Additionally, the switch 111 may allow the user to select an appropriate delay parameter. The signal DIN_DLY may be implemented, in one example, as a delayed data signal. (emphasis added).

Further support is provided on page 9, line 10 through page 10, line 8 of the specification, as originally filed:

> The circuit 100 has been described in the context of the example of two delay elements. However, a number of delay elements may be implemented accordingly to meet the design criteria of a particular implementation. For example, **a plurality of delay elements 109a-109n may be implemented to provide a variety of programmable delay times for the signal DIN_DLY.** In general, particular design parameters may dictate that **a fast or a slow delay time** of the signal DIN_DLY may be required. For example, one of the delay elements 109a-109n may be appropriate to provide timing that may be used with a circuit such as the circuit 10 of FIG. 1. Furthermore, another one of the delay elements 109a-109n may provide a delay of the signal DLY appropriate with a circuit such as the circuit 20 of FIG. 2. Furthermore, another of the delay elements 109a-109n may be programmed

> to provide a delay appropriate for another design application. When the number of delay elements is greater than two, the signal S_H may be implemented as a multi-bit signal. In one example, the signal S_H may be received from an external pin. However, the signal S_H may be received from other sources, such as an internal register, control interface, software instructions, a microprocessor, etc (emphasis added).

Furthermore, a patent need not teach, and preferably omits, what is well known in the art (MPEP §2164.01). Patents may provide evidence of the level of knowledge of one of ordinary skill in the relevant art. The Office Action asserts that the art of record (i.e. Table 2 of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999) shows each of the plurality of delay times is less than a period of the clock signal. Thus, one of ordinary skill in the art would know how to implement and/or set a plurality of delay times that are less than a clock period. Therefore, one reasonably skilled in the art could (i) recognize in the specification a description of the invention defined by the claims and (ii) make or use the claimed invention from the disclosures in the specification coupled with information known in the art without undue experimentation. As such, the Office Action fails to meet the Office's burden to factually establish a reasonable basis to challenge the adequacy of the written description or the enablement provided for the presently claimed invention (see MPEP §§ 2163.04 and 2164.01) and the objection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 1-13 and 15-21 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one of skill in the relevant art that the inventor, at the time of the application was filed, had possession of the claimed invention is respectfully traversed and should be withdrawn.

Since the Office Action merely refers to the reasons set forth in the objection to the specification as the support for the rejection of claims 1-13 and 15-21 under 35 U.S.C. §112, first paragraph (see page 3, paragraph no. 3 of the Office Action), the arguments presented above traversing the objection to the specification are hereby incorporated by reference in support of claims 1-13 and 15-21. For the reasons presented above, the Office Action fails to meet the Office's burden to factually establish a reasonable basis to challenge the adequacy of the written description or the enablement provided by the specification for the presently claimed invention (see MPEP §§ 2163.04 and 2164.01). As such, claims 1-13 and 15-21 are fully patentable under 35 U.S.C. §112, first paragraph and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 11-13 and 21 under 35 U.S.C. §102(a) as being anticipated by Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999 (hereinafter Dallas) has been obviated by appropriate amendment and should be withdrawn.

Dallas disclose a programmable 8-bit silicon delay line (Title).

In contrast, the presently claimed invention (claim 1) provides a first circuit configured to (i) receive a data signal having a first setup/hold window with respect to a clock signal and (ii) present a delayed data signal having a second setup/hold window with respect to said clock signal. A plurality of delay times provides a user configurable delay of the second setup/hold window relative to a transition of the clock signal. Claims 11 and 12 include similar limitations. Assuming, *arguendo*, the signal IN of Dallas is similar to the presently claimed data signal and the signal C of Dallas is similar to the presently claimed clock signal (as suggested in the last four lines on page 3 of the Office Action and for which Applicants' representative does not necessarily agree), Dallas appears to be silent regarding the signal IN having a first setup/hold window with respect to the clock signal C or (ii) the signal OUT of Dallas having a second setup/hold window with respect to the clock signal C, as presently claimed.

Therefore, Dallas does not disclose or suggest each and every element of the present claimed invention, arranged in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, assuming, *arguendo*, the serial input D of Dallas is similar to the presently claimed data signal (a possibility not addressed by the Examiner, but discussed here for completeness), Dallas is silent regarding a configurable delay of a setup/hold window of the serial input D relative to a transition of the clock signal C. Therefore, Dallas does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 3 under 35 U.S.C. §103(a) as being unpatentable over Dallas in view of Brown (US 6,310,506) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 4 under 35 U.S.C. §103(a) as being unpatentable over Dallas in view of JEDEC Standard No. 8-6, "High Speed Transceiver Logic (HSTL) - A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits,"

EIA/JESD8-6, August 1995 (hereinafter JEDEC) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 5-10 and 15-20 under 35 U.S.C. §103(a) as being unpatentable over Dallas in view of JEDEC and in further view of IBM Technical Disclosure Bulletin, "Programmable Delay Line Control Signal Circuits," Vol. 37, No.08, August 1994 (hereinafter IBMTDB) has been obviated by appropriate amendment and should be withdrawn.

Claims 3-10 each depend, either directly or indirectly, on claim 1, which is believed to be allowable. Claims 15-20 each depend, either directly or indirectly, on claim 12, which is also now believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

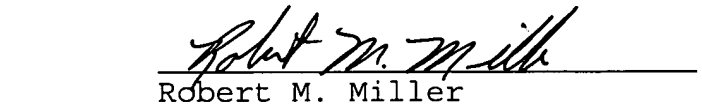
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Robert M. Miller
Registration No. 42,892
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: November 7, 2003

Docket No.: 0325.00355